WHAT IS CLAIMED IS:

1. A method for testing memories with seamless data input/output by interleaving seamless bank commands, comprising the steps of:

transferring data to data input/output (I/O) pins of a memory seamlessly; and

inputting control commands to control pins of the memory seamlessly.

2. The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly inputted to and outputted from the input/output (I/O) pins of the memory.

3. The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly inputted to the input/output (I/O) pins of the memory.

4. The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly outputted from the input/output (I/O) pins of the memory.

5. The method as claimed in claim 1, wherein the memory has at least two banks that have the control pins for receiving the control commands.

6. The method as claimed in claim 1, wherein the memory is a SDRAM, DDR-DRAM or Rambus RDRAM.

7. The method as claimed in claim 1, wherein in the transferring data step, the data are partly masked to purposely achieve a non-seamless status.

8. The method as claimed in claim 1, wherein in the inputting control commands step, the control commands are partly delayed.

9. The method as claimed in claim 1, wherein in the inputting control

commands step, the control commands are partly interrupted.

10. The method as claimed in claim 7, wherein the memory has at least two banks that have the control pins for receiving the control commands.

11. The method as claimed in claim 8, wherein the memory has at least two banks that have the control pins for receiving the control commands.

12. The method as claimed in claim 9, wherein the memory has at least two banks that have the control pins for receiving the control commands.

13. The method as claimed in claim 7, wherein the memory is a SDRAM, DDR-DRAM or Rambus RDRAM.

14. The method as claimed in claim 8, wherein the memory is a SDRAM, DDR-DRAM or Rambus RDRAM.

15. The method as claimed in claim 9, wherein the memory is a SDRAM, DDR-DRAM or Rambus RDRAM.